SILICON N-P-N "overlay" TRANSISTOR

2N5070

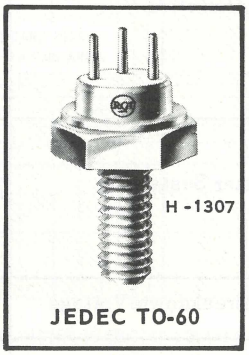
File No. 268

RCA-2N5070* is an epitaxial silicon n-p-n planar transistor of the "overlay" emitter electrode construction. It is especially designed for linear applications to provide high power in Class A or Class B service. This device is intended for 2-to-30 MHz single-sideband power amplifier operating from a 28-volt power supply.

The inherent high frequency capability of the "overlay" structure together with individually ballasted emitter sites makes it possible to forward bias the device into the active region without incurring thermal instability.

The emitter pin is common to case to minimize lead inductance.

Formerly RCA-Dev. No.TA2793



JEDEC TO-60

- For Class-A or Class-B Amplifiers
- For HF Single Sideband Communications
- 25 Watts PEP Output (min.) at 30 MHz
  with Gain: 13 dB (min.)
  η: 40% (min.)
  IMD: 30 dB (max.)
- Low Thermal Resistance

RATINGS

Maximum Ratings, *Absolute-Maximum Values:*

COLECTOR-TO-EMITTER VOLTAGE:			
With V_{BE} = −1.5 V	V_{CEV}	65	V
With external base-to-emitter resistance, R_{BE} = 5 Ω	V_{CER}	40	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	V
COLLECTOR CURRENT:			
Peak		10	A
Continuous	I_C	3.3	A
TRANSISTOR DISSIPATION	P_T		
At case temperatures up to 25° C		70	W
At case temperatures above 25° C		See *Fig.3*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 200	°C
LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. from insulating wafer for 10 s max		230	°C

TYPICAL INTERMODULATION DISTORTION vs. RF POWER OUTPUT

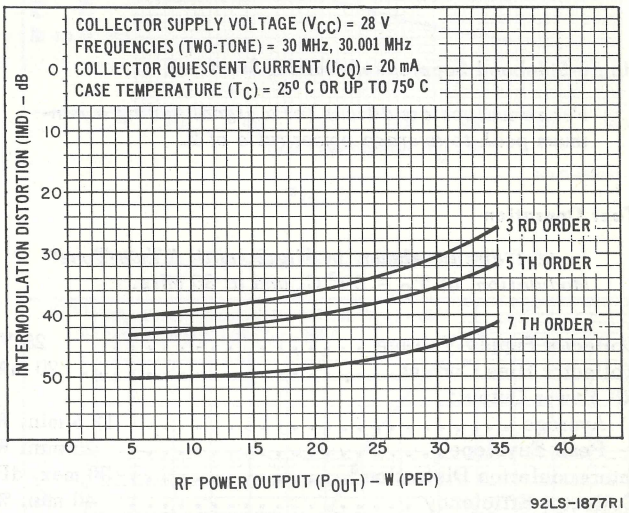


Fig. 1

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ELECTRICAL CHARACTERISTICS
Case Temperature = 25° C

Characteristics	Symbol	TEST CONDITIONS					Limits		Units
		DC Collector Volts		DC Base Volts	DC Current mA				
		V_{CB}	V_{CE}	V_{BE}	I_E	I_C	Min.	Max.	
Collector-to-emitter Sustaining Voltage	$V_{CEV}(sus)$			−1.5		200[a]	65	–	V
	$V_{CER}(sus)$ R_{BE} = 5 Ω					200[a]	40	–	V
Emitter-to-base Breakdown Voltage	BV_{EBO}				10		4	–	V
Collector-to-emitter Cutoff Current	I_{CEO}		30				–	5.0	mA
Collector-to-base Cutoff Current	I_{CBO}	60					–	10	mA
Collector-to-base Capacitance f = 1 MHz	C_{ob}	30					–	85	pF
Junction-to-case Thermal Resistance	θ_{J-C}						–	2.5	°C/W

[a]Pulsed through an inductor (25 mH); duty factor = 50%.

LINEAR RF POWER AMPLIFIER

Single-Sideband Suppressed-Carrier Service

Peak envelope conditions for a signal having a minimum peak-to-average power ratio of 2.

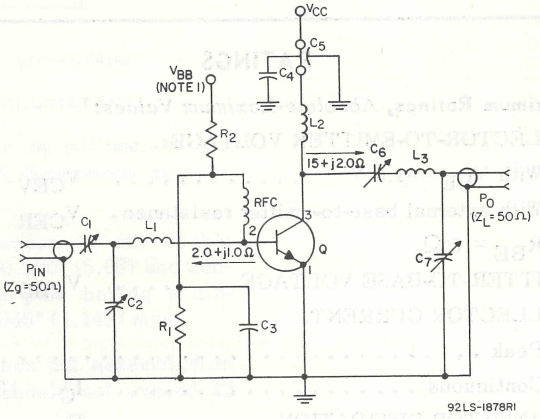
Test Operation

In test circuit shown in Fig.2, with "Two-Tone" Modulation, at T_C = 30° C, and at 30 MHz.

Collector Supply Voltage	28 V
Collector Bias Current	20 mA
RF Power Output:	
Average	12.5 min. W
Peak Envelope	25 min. W
Intermodulation Distortion[a]	30 max. dB
Collector Efficiency	40 min. %

[a]Referenced to either of the two tones and without the use of feedback to enhance linearity.

LINEAR RF AMPLIFIER CIRCUIT FOR POWER OUTPUT TEST (30 MHz Operation)



L_1: 3T No.12 Wire, 1/4" I.D., 1/2" long
L_2: 6T No.14 Wire, 3/8" I.D., 3/4" long
L_3: 5T No.10 Wire, 3/4" I.D., 3/4" long

C_1: 140-680 pF, Arco 468 or equivalent
C_2: 170-780 pF, Arco 469 or equivalent
C_3: 0.05 μF, Ceramic capacitor
C_4: 0.1 μF, Ceramic capacitor
C_5: 1000 pF feedthrough capacitor
C_6: 24-200 pF Arco 425, or equivalent
C_7: 32-250 pF Arco 426, or equivalent

Q: 2N5070
R_1: 1 Ω, 5 W
R_2: 50 Ω, 25 W
RFC: 350 Ferrite choke, Ferroxcube* #VK200 01-03B, or equivalent

*Ferroxcube Corp. of America, Saugerties, N.Y.

Fig. 2

Note 1: Adjust V_{BB} for a collector quiescent current of 20 mA with no RF input signal.

Note 2: Impedance measurements are made at transistor socket pins.

DISSIPATION DERATING CURVE

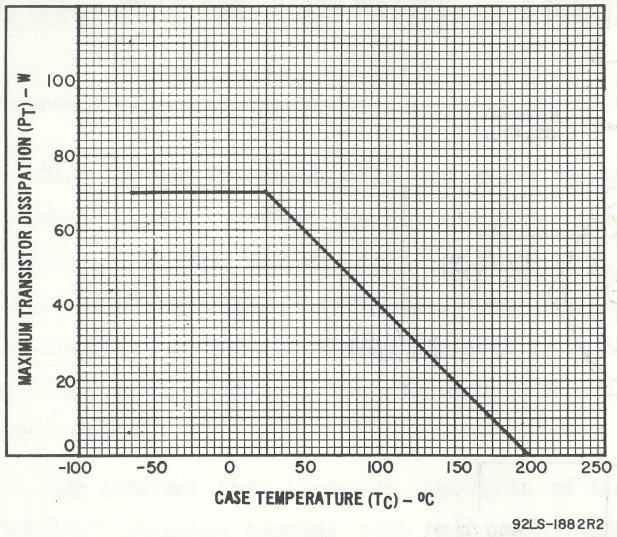


Fig. 3

SAFE OPERATION WITH DC FORWARD BIAS

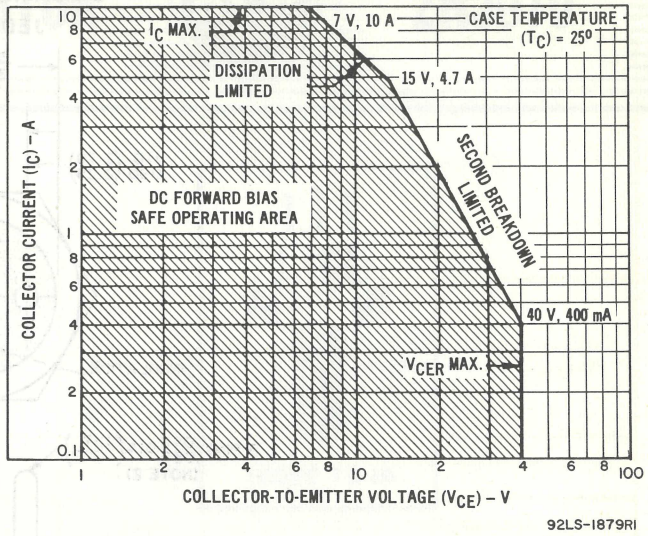


Fig. 4

TYPICAL COLLECTOR EFFICIENCY vs. RF POWER OUTPUT

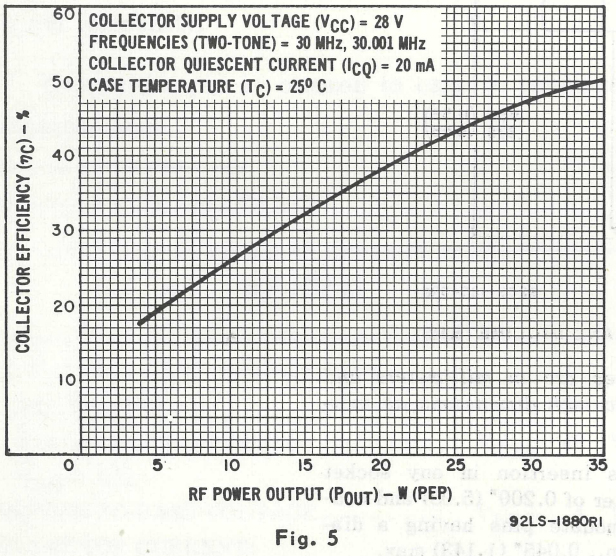


Fig. 5

TYPICAL RF POWER OUTPUT AND INTERMODULATION DISTORTION vs. CASE TEMPERATURE

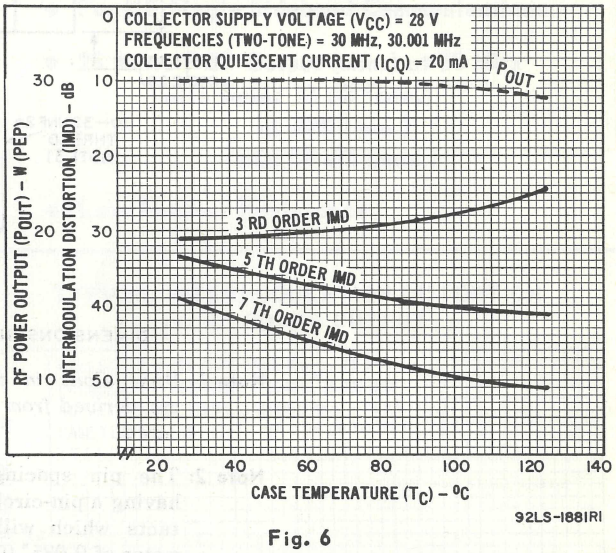


Fig. 6

TYPICAL RF POWER OUTPUT vs. COLLECTOR SUPPLY VOLTAGE

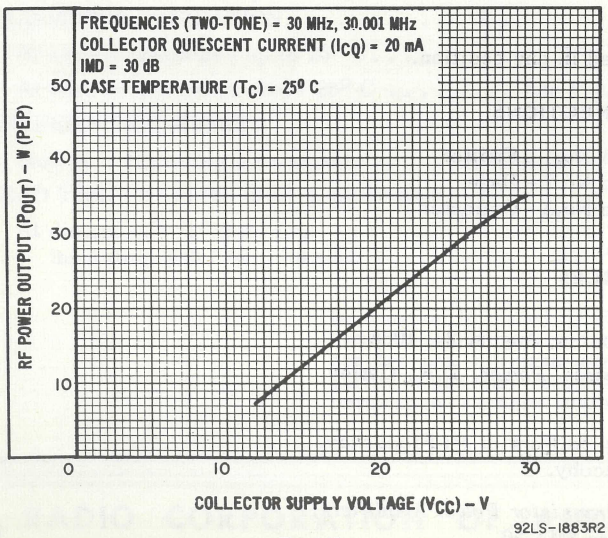


Fig. 7

TYPICAL TRANSFER CHARACTERISTICS

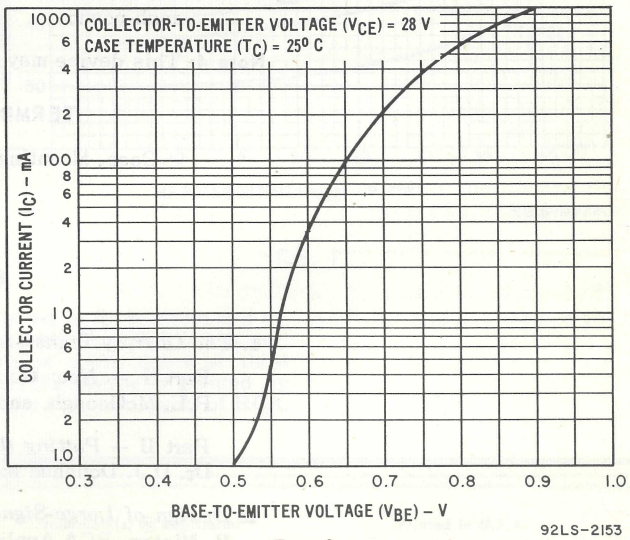
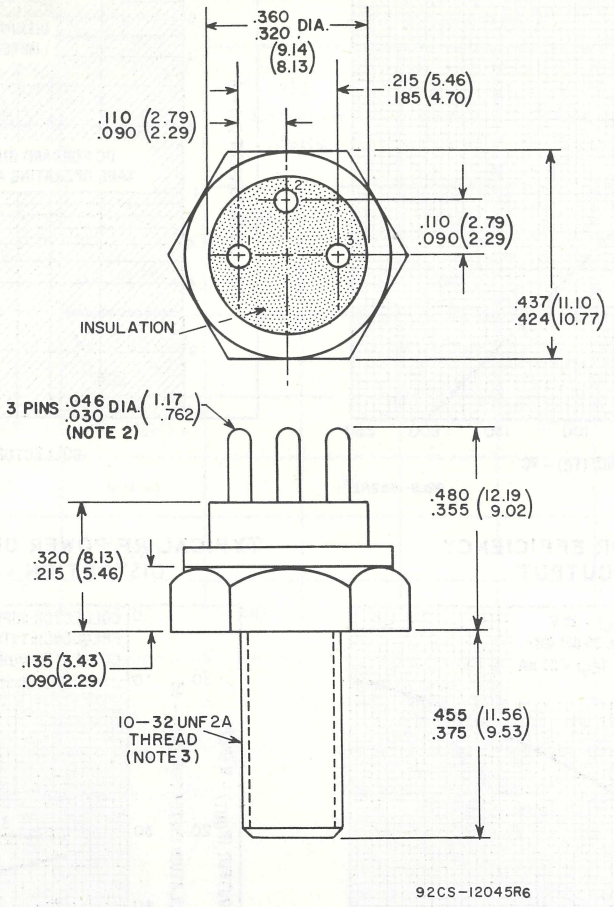


Fig. 8

DIMENSIONAL OUTLINE
JEDEC TO-60



DIMENSIONS IN INCHES AND MILLIMETERS

Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The pin spacing permits insertion in any socket having a pin-circle diameter of 0.200" (5.08) and contacts which will accommodate pins having a diameter of 0.035" (0.889) min., 0.045" (1.143) max.

Note 3: The torque applied to a 10-32 hex nut assembled on the thread during installation should not exceed 12 inch-pounds.

Note 4: This device may be operated in any position.

TERMINAL CONNECTIONS

Case, Mounting Stud, Pin No.1 - Emitter
Pin No.2 - Base
Pin No.3 - Collector

REFERENCES

1. *The Overlay Transistor,* Electronics, August 23, 1965.

Part I – *New Geometry Boosts Power,* D.R. Carley, P.L. McGeough, and J.F. O'Brien.

Part II – *Putting the Overlay to Work at Hi-Frequency,* Dr. D.J. Donahue and B.A. Jacoby.

2. *Design of Large-Signal VHF Transistor Power Amplifiers,* R. Minton, RCA Application Note SMA-36.